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NOTICE OF REASONS FOR REFUSAL

Patent Application Number:	2002-530994
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Examiner:	SAKANIWA Takeshi 9288 5B00
Attorney(s) for applicant:	HONJO Masanori (one other)
Section(s) to be applied:	Sections 29(1), 29(2) and 36

This application should be rejected for the following reasons. If the applicant has any arguments against the reasons, such argument should be submitted within 3 months from the date of shipping of the Notice.

Reasons

1. The inventions in claims 18-32 of the subject application should not be granted a patent under the provision of Patent Law Section 29(1) because of the following reasons.

Note: Regarding claims 18-26, it is not clearly mentioned who or what processes the information mentioned in these claims. If a man processes the information, it is not an "invention" ruled by the Patent Law because the invention uses other than a law of nature. Even if a machine processes the information, it is still unclear how to process the information using the hardware resources.

Regarding claims 27-32, it is described that a certain information processing is performed using hardware resources such as apparatus and registers. However, it is not mentioned about a hardware structure of said hardware resources for performing a certain information processing. Accordingly, the method of information processing using the hardware resources in claims 27-32 is not "concrete."

[The inventions in claims 18-32 have not been examined about the patentability regarding novelty and unobviousness, etc. because the claims are not clear enough to examine.]

2. The subject application does not comply with the requirements under Patent Law Section 36 (6)(ii) on the subject application.

(1) The inventions in claims 1-17 are not clear because the structure of "passes" in claims 1, 2, 12 and 13 is not clearly mentioned.

Note: In the claims, it is mentioned that "a write path to shift an instruction address..." or "a read path to shift an

instruction address..." However, the passes themselves do not have a function to shift an instruction address.

(2) The inventions in claims 3 and 14 are not clear.

Note: The words, "the trace buffer" is considered to cite the words, "the trace buffer circuit." However, the control operation as queue or stack cannot operate only with "registers" and "passes." It should be described clearly about elements that control the "registers" and the "passes."

The meaning of "on the read operation" in the claim 3 is not clear because there are not mentioned about "on the read operation" in the cited claim 1.

(3) The inventions in claims 8-11 are not clear.

Note: "The read path" is not an element in the claim 1. In addition, "register" and "path " are separate elements. Therefore, the meaning of "the first end register on the read path" in claims 8 and 10 is not clear.

(4) The invention in claim 13 is not clear.

Note: The structure of trace buffer circuit connected to the pipelined digital signal processor is described, but an inside structure of said processor is not designated in this claim. Therefore, the structure of "processor" that the applicant wants to obtain a patent is not defined at all.

[Neither novelty nor obviousness is examined about the invention in claim 13 because this invention is not clear enough to examine.]

3. The inventions in the claims listed below of the subject application should not be granted a patent under the provision of Patent Law Section 29(2) since they could have easily been made by persons who have common knowledge in the technical field to which the inventions pertains, on the basis of the inventions described in the publications listed below which were distributed or allowed to use to the public through the electric communication systems in Japan or foreign countries prior to the filing of the subject application.

Notes (The list of cited documents etc. is shown below.)

Claims 1-3: Cited references 1 and 2

The cited reference 1 (See from line 14 of left top column on page 2 to line 6 of right top column on page 2, for example) teaches the invention that writes and then reads a pair of the executed branch instruction address and the branch destination addresses in a memory for tracing 6.

The cited reference 2 (See from line 13 of left top column on page 6 to line 3 of left top column on page 7, for example) teaches to operate stacks formed by a bunch of registers on a first-in first-out mode or a last-in first-out mode.

Since the above cited reference 1 (lines 8-10 of left bottom column on page 3, for example) also teaches that the above memory 6 for tracing is used as a buffer, it is easily created by those skilled in the art to form a trace buffer by a bunch of registers, to operate it so as to shift by two registers as a FIFO register upon writing, and to operate it so as to shift by one register as an LIFO register upon reading.

Claims 4-7 and 15-17: Cited references 1-3

Since the width of the instruction address, the register size, the number of registers, and the value of the bus width are just design matters determined according to the necessity of those skilled in the art, it is an ordinary work for those skilled in the art to adopt any values that are a power of 2.

It is obvious to read out the 32 bit address from the 32 bit read bus. And also it is not difficult for those skilled in the art to form a write bus in 64 bits because the paragraph 12 in the cited reference 3 teaches to store the 64 bit data in the RAM that is formed by merging the jump source address and the jump target address.

Claim 8: Cited references 1-4

The above cited reference 1 (See lines 7-20 of right top column on page 2, and from line 20 of right top column on page 3 to line 1 of left bottom column on page 3, for example) teaches to control that a pair of the instruction address and the branch target address is not written into the memory for tracing when the pair have already resided in the memory. The cited reference 4 (see Figs. 1 and 2, and paragraphs 22-27) discloses a technical idea that sets a pair of addresses compared to a new branch source address and a branch target address to a pair of addresses stored in the register just before that, and generates information at least indicating matching. Accordingly, it is not hard for those skilled in the art to create the structure described in the above claims.

Claim 9: Cited references 1-6

The cited reference 5 (See lines 3-7 of left top column on page 4, lines 1-10 of right top column on page 4, and lines 1-11 of left bottom column on page 4, for example) teaches to write the match output signal (1) in the 1 bit loop flag field

to indicate that the same instruction address is executed again when the program enters a loop operation.

The above cited reference 5 (Fig. 3) discloses that the above loop flag field is provided apart from the address field, while the cited reference 6 (See lines 1-4 of left bottom column on page 3 and from line 1 of right bottom column on page 3 to line 10 of left top column on page 4, for example) discloses a technical idea to apply lower 2 bits of the branch target address to another usage when the branch target address is limited to a multiple of 4. It is not hard for those skilled in the art to create a structure that applies the least significant bit for setting a compression indicator if the branch target address is limited to a multiple of 2.

Claims 10 and 11: Cited references 1-7

The cited reference 7 (See from line 8 of right bottom column on page 3 to line 5 of left top column on page 4, for example) teaches a technical idea to form a plurality of detection circuits for operation that does not trace the results of operation of a loop executing portion with redundancy and also to correspond to the multiple loops.

Portions relating to "state B" described in the above cited reference 2 (from line 14 of right bottom column 5 on page to line 12 of left top column on page 6, etc.) disclose a technical idea that writes into a second pair of registers in a bunch of registers that execute a shift operation. Accordingly, it is not hard for those skilled in the art to set a least significant bit in the branch source address before last and to generate a compression indicator when both addresses match, by comparing a new branch source address to a branch source address before last and comparing a new branch target address to a branch target address before last.

Claim 12: Cited references 1, 2, and 8

The cited reference 8 (See paragraphs 23, 30 and 31, and Fig. 3, for example) teaches to memorize an address of the jump instruction in a trace memory, and to set an effective bit to 1 indicating that the address information is effective corresponding to the memorized address information. It is not hard for those skilled in the art to form a flip-flop for an effective bit and to execute the same control as being connected with a shift control of the trace buffer.

[If any reason(s) for refusal is found later, it will be notified.]

List of Cited References

1. Patent Publication Gazette No. 58-103047
2. Patent Publication Gazette No. 51-050616
3. Patent Publication Gazette No. 05-100900
4. Patent Publication Gazette No. 11-306044
5. Patent Publication Gazette No. 50-120529
6. Patent Publication Gazette No. 02-072440
7. Patent Publication Gazette No. 03-113646
8. Patent Publication Gazette No. 05-324396

Record of the search result of prior technical references

Prior reference(s): Patent Publication No. 08-095824
Patent Publication No. 08-263328

The record of this prior technical reference search is not to show a refusal reason.